APPENDIX A

--98. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to spatial interpolation information generated by the spatial interpolation circuit;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

an image communication link coupled to the resolution reduction circuit, the image communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

a vector communication link coupled to the subpixel vector change circuit, the vector communication link communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit;

a display circuit coupled to the resolution reduction circuit, the display circuit generating display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

a display device coupled to the display circuit, the display device displaying an image in response to the display image information generated by the display circuit.

--99. A system as set forth in claim 98,

wherein the first memory is a first intermediate memory storing the prior pixel image information as intermediate prior pixel image information, and the prior pixel image information representing the prior image;

wherein the second memory is a second intermediate memory storing the next pixel image information as intermediate next pixel image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit is a two dimensional spatial interpolation circuit generating the spatial interpolation information as two dimensional

spatial interpolation information in response to the prior image information stored by the first memory and in response to the next image information stored by the second memory;

wherein the transform processor is a frequency domain transform processor generating the transformed image information as frequency domain transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit is a shaded weight circuit generating the weight information as shaded weight information;

wherein the scale factor circuit is a geometric scale factor circuit generating the scale factor information as geometric scale factor information;

wherein the weighting and scaling circuit is a sum of the products weighting and scaling circuit generating the scaled weighted image information as sum of the products scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit is a fraction removal resolution reduction circuit generating the reduced resolution image information as fraction removal reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link is a digital image communication link communicating the output image information as digital output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link is a digital vector communication link communicating output subpixel vector information in response to the subpixel vector

change information generated by the subpixel vector change circuit as digital output subpixel vector information;

wherein the display circuit is a data decompression display circuit generating the display image information as data decompression display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device is a CRT display device displaying the image as a CRT image in response to the display image information generated by the display circuit.

--100. A system as set forth in claim 98,

wherein the first memory is a first mosaic memory storing the prior pixel image information as prior pixel mosaic image information, and the prior pixel image information representing the prior image;

wherein the second memory is a second mosaic memory storing the next pixel image information as next pixel mosaic image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit is a half pixel resolution spatial interpolation circuit generating the spatial interpolation information as half pixel resolution spatial interpolation information in response to the prior image information stored by the first memory and in response to the next image information stored by the second memory;

wherein the subpixel vector change circuit is an XIP, YIP subpixel vector change circuit generating the subpixel vector change information having subpixel resolution as XIP, YIP vector change information having subpixel resolution in response

to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

wherein the transform processor is a coordinate transform processor generating the transformed image information as coordinate transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit is a weight memory circuit generating the weight information as stored weight information;

wherein the scale factor circuit is a scale factor memory circuit generating the scale factor information as stored scale factor information;

wherein the weighting and scaling circuit is an antialiasing weighting and scaling circuit generating the scaled weighted image information as antialiasing scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit is a truncation resolution reduction circuit generating the reduced resolution image information as truncated reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link is a television image communication link communicating the output image information as television output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link is a television vector communication link communicating output subpixel vector information in response to the

subpixel vector change information generated by the subpixel vector change circuit as television output subpixel vector information;

wherein the display circuit is a composite display circuit generating the display image information as composite display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device is a liquid crystal display device displaying the image as a liquid crystal image in response to the display image information generated by the display circuit.

--101. A system as set forth in claim 98,

wherein the first memory is a first data base memory storing the prior pixel image information, and the prior pixel image information representing the prior image;

wherein the second memory is a second data base memory storing the next pixel image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit is an antialiasing spatial interpolation circuit generating the spatial interpolation information as antialiasing spatial interpolation information in response to the prior image information stored by the first memory and in response to the next image information stored by the second memory;

wherein the subpixel vector change circuit is an initial point subpixel vector change circuit generating the subpixel vector change information having subpixel resolution as initial point vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

wherein the transform processor is a Fourier transform processor generating the transformed image information as Fourier transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit is a subpixel coordinate weight circuit generating the weight information as subpixel coordinate weight information;

wherein the scale factor circuit is a weight scale factor circuit generating the scale factor information as weight scale factor information;

wherein the weighting and scaling circuit is a geometric weighting and scaling circuit generating the scaled weighted image information as geometric scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit is a roundoff resolution reduction circuit generating the reduced resolution image information as rounded off reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link is a data compressed image communication link communicating the output image information as data compressed output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link is a data compressed vector communication link communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit as data compressed output subpixel vector information;

wherein the display circuit is an NTSC display circuit generating the display image information as NTSC display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device is a CRT display device displaying the image as a CRT image in response to the display image information generated by the display circuit.

--102. A system as set forth in claim 98,

wherein the first memory is a first image memory storing the prior pixel image information as eight bit prior pixel image information, and the prior pixel image information representing the prior image;

wherein the second memory is a second image memory storing the next pixel image information as eight bit next pixel image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit is a subpixel resolution spatial interpolation circuit generating the spatial interpolation information as subpixel resolution spatial interpolation information in response to the prior image information stored by the first memory and in response to the next image information stored by the second memory;

wherein the subpixel vector change circuit is an initial condition subpixel vector change circuit generating the subpixel vector change information having subpixel resolution as initial condition vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

wherein the transform processor is a geometric transform processor generating the transformed image information as geometric transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit is a kernel weight circuit generating the weight information as kernel weight information;

wherein the scale factor circuit is a kernel scale factor circuit generating the scale factor information as kernel scale factor information;

wherein the weighting and scaling circuit is a kernel weighting and scaling circuit generating the scaled weighted image information as kernel scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit is an integer resolution reduction circuit generating the reduced resolution image information as integer reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link is a video image communication link communicating the output image information as video output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link is a video vector communication link communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit as video output subpixel vector information;

wherein the display circuit is a red, green, blue display circuit generating the display image information as red, green, blue display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device is a red, green, blue display device displaying the image as a red, green, blue image in response to the display image information generated by the display circuit.

--103. A system as set forth in claim 98,

wherein the first memory is a first memory means for storing the prior pixel image information, and the prior pixel image information representing the prior image;

wherein the second memory is a second memory means for storing the next pixel image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit is a spatial interpolation circuit means for generating the spatial interpolation information in response to the prior image information stored by the first memory and in response to the next image information stored by the second memory;

wherein the subpixel vector change circuit is a subpixel vector change circuit means for generating the subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

wherein the transform processor is a transform processor means for generating the transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit is a weight circuit means for generating the weight information;

wherein the scale factor circuit is a scale factor circuit means for generating the scale factor information;

wherein the weighting and scaling circuit is a weighting and scaling circuit means for generating the scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit is a resolution reduction circuit means for generating the reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link is an image communication link means for communicating the output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link is a vector communication link means for communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit;

wherein the display circuit is a display circuit means for generating the display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device is a display device means for displaying the image in response to the display image information generated by the display circuit.

--104. A system comprising:

a first storing means for storing prior pixel image information, the first storing means storing the prior pixel image information, the prior pixel image information representing a prior image;

a second storing means for storing next pixel image information, the second storing means storing the next pixel image information, the next pixel image information representing a next image;

a first generating means for generating spatial interpolation information in response to the prior pixel image information stored by the first storing means and in response to the next pixel image information stored by the second storing means;

a second generating means for generating subpixel vector change information having subpixel resolution in response to the prior pixel image information

stored by the first storing means and in response to the next pixel image information stored by the second storing means;

a third generating means for generating transformed image information in response to the spatial interpolation information generated by the first generating means;

a fourth generating means for generating weight information;

a fifth generating means for generating scale factor information;

a sixth generating means for generating scaled weighted image information in response to the transformed image information generated by the third generating means, in response to the scale factor information generated by the fifth generating means, and in response to the weight information generated by the fourth generating means;

a seventh generating means for generating reduced resolution image information in response to the scaled weighted image information generated by the sixth generating;

a first communicating means for communicating output image information in response to the reduced resolution image information generated by the seventh generating means;

a second communicating means for communicating output subpixel vector information in response to the subpixel vector change information generated by the second generating means;

an eighth generating means for generating display image information in response to the reduced resolution image information generated by the seventh generating means; and

a displaying means for displaying an image in response to the display image information generated by the eighth generating means.

--105. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to spatial interpolation information generated by the spatial interpolation circuit.

--106. A system as set forth in claim 105, further comprising:

a communication link coupled to the transform processor, the communication link communicating output image information in response to the transformed image information generated by the transform processor.

--107. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--108. A system as set forth in claim 107, further comprising:

a communication link coupled to the spatial interpolation circuit, the communication link communicating output image information in response to the spatial interpolation information generated by the spatial interpolation circuit.

--109. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image; and

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--110. A system as set forth in claim 109, further comprising:

a communication link coupled to the first memory and coupled to the second memory, the communication link communicating output image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--111. A system as set forth in claim 109, further comprising:

a communication link coupled to the subpixel vector change circuit and communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit.

--112. A system as set forth in claim 109, further comprising:

a display circuit coupled to the first memory and coupled to the second memory and generating display image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

a display device coupled to the display circuit and displaying an image in response to the display image information generated by the display circuit.

--113. A system comprising:

a subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image.

--114. A system as set forth in claim 113, further comprising:

a communication link coupled to the subpixel vector change circuit and communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit.

--115. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image; and

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--116. A system as set forth in claim 115, further comprising:

a communication link coupled to the spatial interpolation circuit, the communication link communicating output image information in response to the spatial interpolation information generated by the spatial interpolation circuit.

--117. A system comprising:

a spatial interpolation circuit generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image.

--118. A system as set forth in claim 117, further comprising:

a communication link coupled to the spatial interpolation circuit, the communication link communicating output image information in response to the spatial interpolation information generated by the spatial interpolation circuit.

--119. A system as set forth in claim 117, further comprising:

a communication link communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information in response to the next pixel image information.

--120. A system as set forth in claim 117, further comprising:

a display circuit coupled to the spatial interpolation circuit and generating display image information in response to the spatial interpolation information generated by the spatial interpolation circuit; and

a display device coupled to the display circuit and displaying an image in response to the display image information generated by the display circuit.

--121. A system comprising:

a spatial interpolation circuit generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image; and

a subpixel vector change circuit generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information.

--122. A system as set forth in claim 121, further comprising:

a communication link coupled to the spatial interpolation circuit, the communication link communicating output image information in response to the spatial interpolation information generated by the spatial interpolation circuit.

--123. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

a transform processor coupled to the first memory and coupled to the second memory, the transform processor generating transformed image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--124. A system as set forth in claim 123, further comprising:

a communication link coupled to the transform processor, the communication link communicating output image information in response to the transformed image information generated by the transform processor.

--125. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image; and

a transform processor coupled to the first memory and coupled to the second memory, the transform processor generating transformed image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--126. A system as set forth in claim 125, further comprising:

a communication link coupled to the transform processor, the communication link communicating output image information in response to the transformed image information generated by the transform processor.

--127. A system comprising:

a transform processor generating transformed image information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image.

--128. A system as set forth in claim 127, further comprising:

a communication link coupled to the transform processor, the communication link communicating output image information in response to the transformed image information generated by the transform processor.

--129. A system as set forth in claim 127, further comprising:

a communication link communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information in response to the next pixel image information.

--130. A system as set forth in claim 127, further comprising:

a display circuit coupled to the transform processor and generating display image information in response to the transformed image information generated by the transform processor; and

a display device coupled to the display circuit and displaying an image in response to the display image information generated by the display circuit.

--131. A system comprising:

a subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image; and

a transform processor generating transformed image information in response to the prior pixel image information and in response to the next pixel image information.

--132. A system as set forth in claim 131, further comprising:

a communication link coupled to the transform processor, the communication link communicating output image information in response to the transformed image information generated by the transform processor.

--133. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to spatial interpolation information generated by the spatial interpolation circuit.

--134. A system as set forth in claim 133, further comprising:

a communication link coupled to the transform processor, the communication link communicating output image information in response to the transformed image information generated by the transform processor.

--135. A system comprising:

a spatial interpolation circuit generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image; and

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to spatial interpolation information generated by the spatial interpolation circuit.

--136. A system as set forth in claim 135, further comprising:

a communication link coupled to the transform processor, the communication link communicating output image information in response to the transformed image information generated by the transform processor.

--137. A system comprising:

a spatial interpolation circuit generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

a subpixel vector change circuit generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information; and

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to spatial interpolation information generated by the spatial interpolation circuit.

--138. A system as set forth in claim 137, further comprising:

a communication link coupled to the transform processor, the communication link communicating output image information in response to the transformed image information generated by the transform processor.

--139. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the spatial interpolation circuit, the weighting and scaling circuit generating scaled weighted image information in response to the spatial interpolation information generated by the spatial interpolation circuit, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit.

--140. A system as set forth in claim 139, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--141. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, coupled to the first memory and coupled to the second memory, the weighting and scaling circuit generating scaled weighted image in response to the prior pixel image information stored by the first memory, in response to the next pixel image information stored by the second memory, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in

response to the scaled weighted image information generated by the weighting and scaling circuit.

--142. A system as set forth in claim 141, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--143. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, coupled to the first memory and coupled to the second memory, the weighting and scaling circuit generating scaled weighted image in response to the prior pixel image information stored by the first memory, in response to the next pixel image information stored by the second memory, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit.

--144. A system as set forth in claim 143, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--145. A system comprising:

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit and coupled to the weight circuit, the weighting and scaling circuit generating scaled weighted image in response to prior pixel image information, in response to next pixel image information, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit, the prior pixel image information representing a prior image and the next pixel image information representing a next image; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit.

--146. A system as set forth in claim 145, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--147. A system as set forth in claim 145, further comprising:

a communication link communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information in response to the next pixel image information.

--148. A system as set forth in claim 145, further comprising:

a display circuit coupled to the resolution reduction circuit, the display circuit generating display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

a display device coupled to the display circuit, the display device displaying an image in response to the display image information generated by the display circuit.

--149. A system comprising:

a subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit and coupled to the weight circuit, the weighting and scaling circuit generating scaled weighted image in response to the prior pixel image information, in response to the next pixel image information, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in

response to the scaled weighted image information generated by the weighting and scaling circuit.

--150. A system as set forth in claim 149, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--151. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the spatial interpolation circuit, the weighting and scaling circuit generating scaled weighted image information in response to the spatial interpolation information generated by the spatial interpolation circuit, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in

response to the scaled weighted image information generated by the weighting and scaling circuit.

--152. A system as set forth in claim 151, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--153. A system comprising:

a spatial interpolation circuit generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the spatial interpolation circuit, the weighting and scaling circuit generating scaled weighted image information in response to the spatial interpolation information generated by the spatial interpolation circuit, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit.

--154. A system as set forth in claim 153, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--155. A system comprising:

a spatial interpolation circuit generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

a subpixel vector change circuit generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the spatial interpolation circuit, the weighting and scaling circuit generating scaled weighted image information in response to the spatial interpolation information generated by the spatial interpolation circuit, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit.

--156. A system as set forth in claim 155, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--157. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a transform processor coupled to the first memory and coupled to the second memory, the transform processor generating transformed image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit.

--158. A system as set forth in claim 157, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--159. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a transform processor coupled to the first memory and coupled to the second memory, the transform processor generating transformed image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit.

--160. A system as set forth in claim 159, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--161. A system comprising:

a transform generating transformed image information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit.

--162. A system as set forth in claim 161, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--163. A system comprising:

a subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

a transform processor generating transformed image information in response to the prior pixel image information and in response to the next pixel image information;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit.

--164. A system as set forth in claim 163, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--165. A system comprising:

a first memory storing prior pixel image information, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to spatial interpolation information generated by the spatial interpolation circuit;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in

response to the scaled weighted image information generated by the weighting and scaling circuit.

--166. A system as set forth in claim 165, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--167. A system comprising:

a spatial interpolation circuit generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to spatial interpolation information generated by the spatial interpolation circuit;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in

response to the scaled weighted image information generated by the weighting and scaling circuit.

--168. A system as set forth in claim 167, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--169. A system comprising:

a spatial interpolation circuit generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

a subpixel vector change generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information;

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to spatial interpolation information generated by the spatial interpolation circuit;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit; and

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit.

--170. A system as set forth in claim 169, further comprising:

a communication link coupled to the resolution reduction circuit, the communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--171. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating transformed image information in response to spatial interpolation information;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--172. A process as set forth in claim 171, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--173. A process as set forth in claim 171, further comprising the act of:

communicating output subpixel vector information in response to the subpixel vector change information.

--174. A process as set forth in claim 171, further comprising the acts of:

generating display image information in response to the reduced resolution image information; and

displaying an image in response to the display image information.

--175. A process as set forth in claim 171, further comprising the act of:

making a product in response to the reduced resolution image information.

--176. A process as set forth in claim 171, further comprising the act of:

making an information product in response to the reduced resolution image information.

--177. A process as set forth in claim 171, further comprising the act of:

making an entertainment product in response to the reduced resolution image information.

--178. A process as set forth in claim 171, further comprising the act of:

making a physical product in response to the reduced resolution image information.

--179. A process as set forth in claim 171, further comprising the act of:

making a designed product in response to the reduced resolution image information.

--180. A process as set forth in claim 171, further comprising the act of:

making a manufactured product in response to the reduced resolution image information.

--181. A process as set forth in claim 171, further comprising the act of:

making a processed product in response to the reduced resolution image information.

--182. A process as set forth in claim 171, further comprising the act of:

making a training product in response to the reduced resolution image information.

--183. A process as set forth in claim 171, further comprising the act of:

making an oil product in response to the reduced resolution image information.

--184. A process as set forth in claim 171, further comprising the act of:

making a mineral product in response to the reduced resolution image information.

--185. A process as set forth in claim 171, further comprising the act of:

making an electronic product in response to the reduced resolution image information.

--186. A process as set forth in claim 171, further comprising the act of:

making an architectural product in response to the reduced resolution image information.

--187. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image

information stored by the first memory and in response to the next pixel image information stored by the second memory; and

generating transformed image information in response to spatial interpolation information.

--188. A process as set forth in claim 187, further comprising the act of:

communicating output image information in response to the spatial interpolation information.

--189. A process as set forth in claim 187, further comprising the act of:

making a product in response to the spatial interpolation information.

--190. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--191. A process as set forth in claim 190, further comprising the act of:

communicating output image information in response to the spatial interpolation information.

--192. A process as set forth in claim 190, further comprising the act of:

making a product in response to the spatial interpolation information.

--193. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image; and

generating subpixel vector change information generated by the subpixel vector change circuit having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--194. A process as set forth in claim 193, further comprising the act of:

communicating output image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--195. A process as set forth in claim 193, further comprising the act of:

communicating output subpixel vector information in response to the subpixel vector change information.

--196. A process as set forth in claim 193, further comprising the acts of:

generating display image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

displaying an image in response to the display image information.

--197. A process as set forth in claim 193, further comprising the act of:

making a product in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--198. A process comprising the acts of:

generating subpixel vector change information having subpixel resolution in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image.

--199. A process as set forth in claim 198, further comprising the act of:

communicating output subpixel vector information in response to the subpixel vector change information.

--200. A process as set forth in claim 198, further comprising the act of:

making a product in response to the subpixel vector change information.

--201. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image; and

generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--202. A process as set forth in claim 201, further comprising the act of:

communicating output image information in response to the spatial interpolation information.

--203. A process as set forth in claim 201, further comprising the act of:

making a product in response to the spatial interpolation information.

--204. A process comprising the acts of:

generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image.

--205. A process as set forth in claim 204, further comprising the act of:

communicating output image information in response to the spatial interpolation information.

--206. A process as set forth in claim 204, further comprising the act of:

communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information in response to the next pixel image information.

--207. A process as set forth in claim 204, further comprising the acts of:

generating display image information in response to the spatial interpolation information; and

displaying an image in response to the display image information.

--208. A process as set forth in claim 204, further comprising the act of:

making a product in response to the spatial interpolation information.

--209. A process comprising the acts of:

generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image; and

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information.

--210. A process as set forth in claim 209, further comprising the act of:

communicating output image information in response to the spatial interpolation information.

--211. A process as set forth in claim 209, further comprising the act of:

making a product in response to the spatial interpolation information.

--212. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

generating transformed image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--213. A process as set forth in claim 212, further comprising the act of:

communicating output image information in response to the transformed image information.

--214. A process as set forth in claim 212, further comprising the act of:

making a product in response to the transformed image information.

--215. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image; and

generating transformed image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory.

--216. A process as set forth in claim 215, further comprising the act of:

communicating output image information in response to the transformed image information.

--217. A process as set forth in claim 215, further comprising the act of:

making a product in response to the transformed image information.

--218. A process comprising the acts of:

generating transformed image information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image.

--219. A process as set forth in claim 218, further comprising the act of:

communicating output image information in response to the transformed image information.

--220. A process as set forth in claim 218, further comprising the act of:

communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information in response to the next pixel image information.

--221. A process as set forth in claim 218, further comprising the acts of:

generating display image information in response to the transformed image information; and

displaying an image in response to the display image information.

--222. A process as set forth in claim 218, further comprising the act of:

making a product in response to the transformed image information.

--223. A process comprising the acts of:

generating subpixel vector change information having subpixel resolution in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image; and

generating transformed image information in response to the prior pixel image information and in response to the next pixel image information.

--224. A process as set forth in claim 223, further comprising the act of:

communicating output image information in response to the transformed image information.

--225. A process as set forth in claim 223, further comprising the act of:

making a product in response to the transformed image information.

--226. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory; and

generating transformed image information in response to spatial interpolation information.

--227. A process as set forth in claim 226, further comprising the act of:

communicating output image information in response to the transformed image information.

--228. A process as set forth in claim 226, further comprising the act of:

making a product in response to the transformed image information.

--229. A process comprising the acts of:

generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image; and

generating transformed image information in response to spatial interpolation information.

--230. A process as set forth in claim 229, further comprising the act of:

communicating output image information in response to the transformed image information.

--231. A process as set forth in claim 229, further comprising the act of:

making a product in response to the transformed image information.

--232. A process comprising the acts of:

generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information; and

generating transformed image information in response to spatial interpolation information.

--233. A process as set forth in claim 232, further comprising the act of:

communicating output image information in response to the transformed image information.

--234. A process as set forth in claim 232, further comprising the act of:

making a product in response to the transformed image information.

--235. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the spatial interpolation information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

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--236. A process as set forth in claim 235, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--237. A process as set forth in claim 235, further comprising the act of:

making a product in response to the reduced resolution image information.

--238. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating weight information;

generating scale factor information;

generating scaled weighted image in response to the prior pixel image information stored by the first memory, in response to the next pixel image information stored by the second memory, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--239. A process as set forth in claim 238, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--240. A process as set forth in claim 238, further comprising the act of:

making a product in response to the reduced resolution image information.

--241. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating weight information;

generating scale factor information;

generating scaled weighted image in response to the prior pixel image information stored by the first memory, in response to the next pixel image information stored by the second memory, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--242. A process as set forth in claim 241, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--243. A process as set forth in claim 241, further comprising the act of:

making a product in response to the reduced resolution image information.

--244. A process comprising the acts of:

generating weight information;

generating scale factor information;

generating scaled weighted image in response to prior pixel image information, in response to next pixel image information, in response to the scale factor information, and in response to the weight information, the prior pixel image information representing a prior image and the next pixel image information representing a next image; and

generating reduced resolution image information in response to the scaled weighted image information.

--245. A process as set forth in claim 244, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--246. A process as set forth in claim 244, further comprising the act of:

communicating output prior pixel image information in response to the prior pixel image information and communicating output next pixel image information in response to the next pixel image information.

--247. A process as set forth in claim 244, further comprising the acts of:

generating display image information in response to the reduced resolution image information; and

displaying an image in response to the display image information.

--248. A process as set forth in claim 244, further comprising the act of:

making a product in response to the reduced resolution image information.

--249. A process comprising the acts of:

generating subpixel vector change information having subpixel resolution in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

generating weight information;

generating scale factor information;

generating scaled weighted image in response to the prior pixel image information, in response to the next pixel image information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--250. A process as set forth in claim 249, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--251. A process as set forth in claim 249, further comprising the act of:

making a product in response to the reduced resolution image information.

--252. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the spatial interpolation information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--253. A process as set forth in claim 252, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--254. A process as set forth in claim 252, further comprising the act of:

making a product in response to the reduced resolution image information.

--255. A process comprising the acts of:

generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the spatial interpolation information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--256. A process as set forth in claim 255, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--257. A process as set forth in claim 255, further comprising the act of:

making a product in response to the reduced resolution image information.

--258. A process comprising the acts of:

generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the spatial interpolation information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--259. A process as set forth in claim 258, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--260. A process as set forth in claim 258, further comprising the act of:

making a product in response to the reduced resolution image information.

--261. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating transformed image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--262. A process as set forth in claim 261, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--263. A process as set forth in claim 261, further comprising the act of:

making a product in response to the reduced resolution image information.

--264. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating transformed image information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--265. A process as set forth in claim 264, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--266. A process as set forth in claim 264, further comprising the act of:

making a product in response to the reduced resolution image information.

--267. A process comprising the acts of:

a transform generating transformed image information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--268. A process as set forth in claim 267, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--269. A process as set forth in claim 267, further comprising the act of:

making a product in response to the reduced resolution image information.

--270. A process comprising the acts of:

generating subpixel vector change information having subpixel resolution in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

generating transformed image information in response to the prior pixel image information and in response to the next pixel image information;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--271. A process as set forth in claim 270, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--272. A process as set forth in claim 270, further comprising the act of:

making a product in response to the reduced resolution image information.

--273. A process comprising the acts of:

storing prior pixel image information in a first memory, the prior pixel image information representing a prior image;

storing next pixel image information in a second memory, the next pixel image information representing a next image;

generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

generating transformed image information in response to spatial interpolation information;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--274. A process as set forth in claim 273, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--275. A process as set forth in claim 273, further comprising the act of:

making a product in response to the reduced resolution image information.

--276. A process comprising the acts of:

generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

generating transformed image information in response to spatial interpolation information;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--277. A process as set forth in claim 276, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--278. A process as set forth in claim 276, further comprising the act of:

making a product in response to the reduced resolution image information.

--279. A process comprising the acts of:

generating spatial interpolation information in response to prior pixel image information, the prior pixel image information representing a prior image, and in response to next pixel image information, the next pixel image information representing a next image;

generating subpixel vector change information having subpixel resolution in response to the prior pixel image information and in response to the next pixel image information;

generating transformed image information in response to spatial interpolation information;

generating weight information;

generating scale factor information;

generating scaled weighted image information in response to the transformed image information, in response to the scale factor information, and in response to the weight information; and

generating reduced resolution image information in response to the scaled weighted image information.

--280. A process as set forth in claim 279, further comprising the act of:

communicating output image information in response to the reduced resolution image information.

--281. A process as set forth in claim 279, further comprising the act of:

making a product in response to the reduced resolution image information.

--282. A display system as set forth in claim 97, wherein the display processor comprises:

a first memory coupled to the memory and storing prior pixel image information in response to the image stored in the memory, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to spatial interpolation information generated by the spatial interpolation circuit;

a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed

image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

an image communication link coupled to the resolution reduction circuit, the image communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

a vector communication link coupled to the subpixel vector change circuit, the vector communication link communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit; and

a display circuit coupled to the resolution reduction circuit, the display circuit generating the scanned out image in response to the reduced resolution image information generated by the resolution reduction circuit.

--283. A display system comprising:

a memory storing an image;

a first memory coupled to the memory and storing prior pixel image information in response to the image stored in the memory, the prior pixel image information representing a prior image;

a second memory storing next pixel image information, the next pixel image information representing a next image;

a spatial interpolation circuit coupled to the first memory and coupled to the second memory, the spatial interpolation circuit generating spatial interpolation

information in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a subpixel vector change circuit coupled to the first memory and coupled to the second memory, the subpixel vector change circuit generating subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

a transform processor coupled to the spatial interpolation circuit, the transform processor generating transformed image information in response to spatial interpolation information generated by the spatial interpolation circuit;

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a weight circuit generating weight information;

a scale factor circuit generating scale factor information;

a weighting and scaling circuit coupled to the scale factor circuit, coupled to the weight circuit, and coupled to the transform processor, the weighting and scaling circuit generating scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

a resolution reduction circuit coupled to the weighting and scaling circuit, the resolution reduction circuit generating reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

an image communication link coupled to the resolution reduction circuit, the image communication link communicating output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

a vector communication link coupled to the subpixel vector change circuit, the vector communication link communicating output subpixel vector information in

response to the subpixel vector change information generated by the subpixel vector change circuit;

a display processor coupled to the memory and coupled to the resolution reduction circuit, the display processor scanning out the image stored in the memory in response to the reduced resolution image information generated by the resolution reduction circuit; and

a display medium coupled to the display processor and displaying the image scanned out by the display processor.

--284. A system as set forth in claim 98,

wherein the spatial interpolation circuit includes a spatial interpolation processor circuit for generating the spatial interpolation information in response to the prior image information stored by the first memory and in response to the next image information stored by the second memory;

wherein the subpixel vector change circuit includes a subpixel vector change processor circuit generating the subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

wherein the weight circuit includes a weight processor circuit for generating the weight information;

wherein the scale factor circuit includes a scale factor processor circuit for generating the scale factor information;

wherein the weighting and scaling circuit includes a weighting and scaling processor circuit for generating the scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the

scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit includes a resolution reduction processor circuit for generating the reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit; and

wherein the display circuit includes a display processor circuit for generating the display image information in response to the reduced resolution image information generated by the resolution reduction circuit.

--285. A system as set forth in claim 98,

wherein the first memory includes a plurality of first memories for storing the prior pixel image information, and the prior pixel image information representing the prior image;

wherein the second memory includes a plurality of second memories for storing the next pixel image information, the second memory storing the next pixel image information and the next pixel image information representing the next image;

wherein the spatial interpolation circuit includes a plurality of spatial interpolation circuits for generating the spatial interpolation information in response to the prior image information stored by the first memory and in response to the next image information stored by the second memory;

wherein the subpixel vector change circuit includes a plurality of subpixel vector change circuits for generating the subpixel vector change information having subpixel resolution in response to the prior pixel image information stored by the first memory and in response to the next pixel image information stored by the second memory;

wherein the transform processor includes a plurality of transform processors for generating the transformed image information in response to the spatial interpolation information generated by the spatial interpolation circuit;

wherein the weight circuit includes a plurality of weight circuits for generating the weight information;

wherein the scale factor circuit includes a plurality of scale factor circuits for generating the scale factor information;

wherein the weighting and scaling circuit includes a plurality of weighting and scaling circuits for generating the scaled weighted image information in response to the transformed image information generated by the transform processor, in response to the scale factor information generated by the scale factor circuit, and in response to the weight information generated by the weight circuit;

wherein the resolution reduction circuit includes a plurality of resolution reduction circuits for generating the reduced resolution image information in response to the scaled weighted image information generated by the weighting and scaling circuit;

wherein the image communication link includes a plurality of image communication links for communicating the output image information in response to the reduced resolution image information generated by the resolution reduction circuit;

wherein the vector communication link includes a plurality of vector communication links for communicating output subpixel vector information in response to the subpixel vector change information generated by the subpixel vector change circuit;

wherein the display circuit includes a plurality of display circuits for generating the display image information in response to the reduced resolution image information generated by the resolution reduction circuit; and

wherein the display device includes a plurality of display devices for displaying the image in response to the display image information generated by the display circuit.

--286. A system as set forth in claim 98,

wherein the weighting and scaling circuit comprises:

a weighting circuit coupled to the weight circuit and coupled to the transform processor, the weighting circuit generating weighted image information in response to the weight information generated by the weight circuit and in response to the transformed image information generated by the transform processor; and

a scaling circuit coupled to the scale factor circuit and coupled to the weighting circuit, the scaling circuit generating the weighted scaled image information in response to the scale factor information generated by the scale factor circuit and in response to the weighted image information generated by the weighting circuit.

--287. A system as set forth in claim 98,

wherein the weighting and scaling circuit comprises:

a scaling circuit coupled to the scale factor circuit and coupled to the transform processor, the scaling circuit generating scaled image information in response to the scale factor information generated by the scale factor circuit and in response to the transformed image information generated by the transform processor; and

a weighting circuit coupled to the weight circuit and coupled to the scaling circuit, the weighting circuit generating the weighted scaled image information in response to the weight information generated by the weight circuit and in response to the scaled image information generated by the scaling circuit.

--288. A system as set forth in claim 98,

wherein the weighting and scaling circuit is a simultaneous weighting and scaling circuit simultaneously generating the weighted scaled image information in response to the weighting information generated by the weighting circuit, in response to

the scale factor information generated by the scale factor circuit and in response to the transformed image information generated by the transform processor.

--289. A system as set forth in claim 98,

wherein the weighting and scaling circuit comprises:

a weighting circuit coupled to the weight circuit and coupled to the input circuit, the weighting circuit generating weighted image information in response to the weight information generated by the weight circuit and in response to the blocks of input image information generated by the input circuit; and

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a scaling circuit coupled to the scale factor circuit and coupled to the weighting circuit, the scaling circuit generating the weighted scaled image information in response to the scale factor information generated by the scale factor circuit and in response to the weighted image information generated by the weighting circuit.

--290. A system as set forth in claim 98,

wherein the weighting and scaling circuit comprises:

a scaling circuit coupled to the scale factor circuit and coupled to the input circuit, the scaling circuit generating scaled image information in response to the scale factor information generated by the scale factor circuit and in response to the blocks of input image information generated by the input circuit; and

a weighting circuit coupled to the weight circuit and coupled to the scaling circuit, the weighting circuit generating the weighted scaled image information in response to the weight information generated by the weight circuit and in response to the scaled image information generated by the scaling circuit.

--291. A system as set forth in claim 98,

wherein the weighting and scaling circuit is a simultaneous weighting and scaling circuit simultaneously generating the weighted scaled image information in response to the weighting information generated by the weighting circuit, in response to the scale factor information generated by the scale factor circuit and in response to the blocks of input image information generated by the input circuit.